

Doc. Number:

- ☐ Tentative Specification
☒ Preliminary Specification
☐ Approval Specification

MODEL NO.: N156DCE
SUFFIX: GN2 Rev.C1

Customer:**APPROVED BY****SIGNATURE**Name / Title

Note

Please return 1 copy for your confirmation with your
signature and comments.

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
1.0	Sep. 6, 2017	All	Spec Ver.1.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156DCE-GN2 is a 15.6" TFT Liquid Crystal Display NB module with LED Backlight unit and 40 pins eDP interface. This module supports 3840 x 2160 UHD mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	15.6" diagonal	-	-
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch	0.2988 (H) x 0.2988 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Anti-Glare(3H)	-	-
Color Gamut	Adobe 100%	NTSC	-
Luminance, White	600	Cd/m2	-
Power Consumption	Total (13.28)W (Max.) @ Cell (1.65)W (Max.), BL (11.63)W (Max.)		(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, $f_v = 60$ Hz, LED_VCCS = Typ, $f_{PWM} = 200$ Hz, Duty=100% and $T_a = 25 \pm 2$ °C, whereas Mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	350.36	350.66	350.96	mm	(1)(2)
	Vertical (V)	216.82	217.32	217.82	mm	
	Thickness (T)	-	2.45	2.60	mm	
Bezel Area	Horizontal	350.36	350.66	350.96	mm	-
	Vertical	205.24	205.54	205.84	mm	-
Active Area	Horizontal	344.12	344.22	344.32	mm	-
	Vertical	193.52	193.62	193.72	mm	-
Glass Thickness	CF	0.25	0.3	0.35	mm	-
	TFT	0.25	0.3	0.35	mm	-
Weight		-	305	320	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) dimensions are measured by caliper

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12.

User's connector Part No: IPEX-20453-040T-03.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

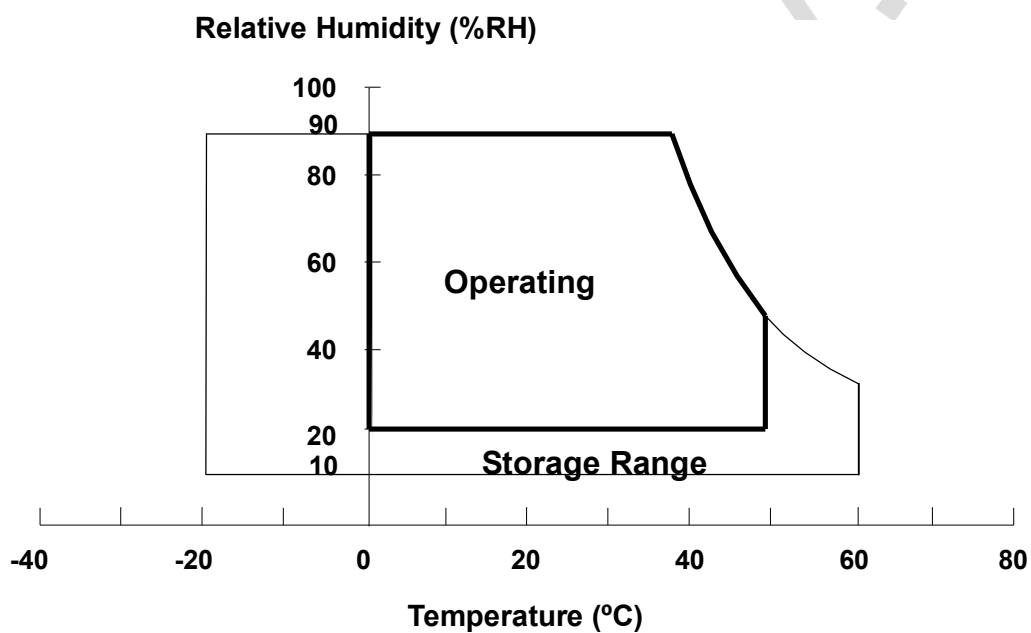
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 °C).

(b) Wet-bulb temperature should be 39 °C Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



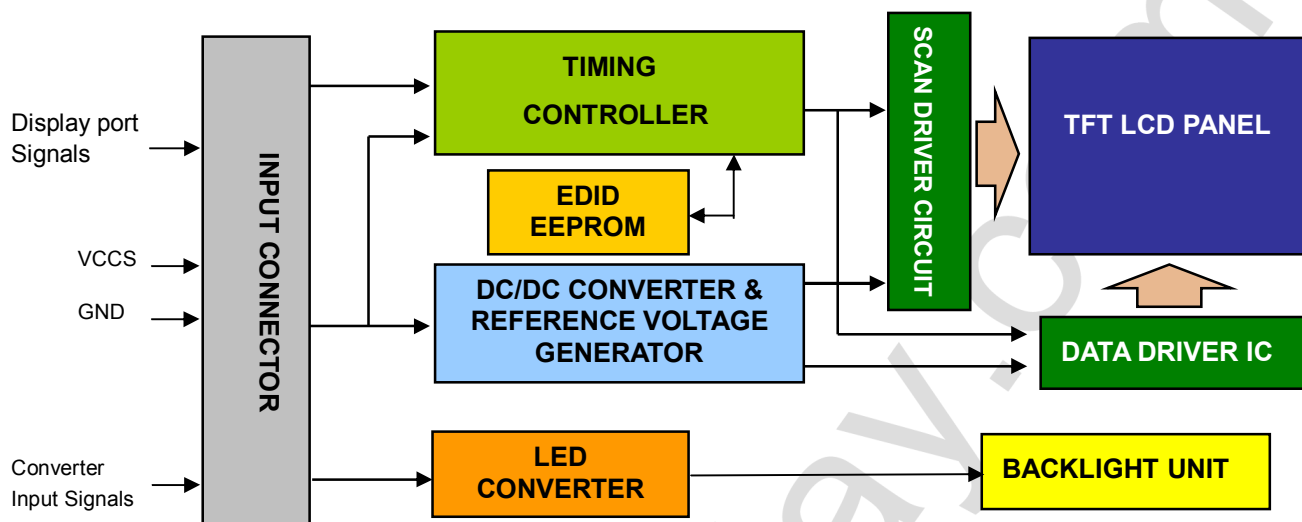
3.2 ELECTRICAL ABSOLUTE RATINGS**3.2.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	+4.0	V	(1)
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



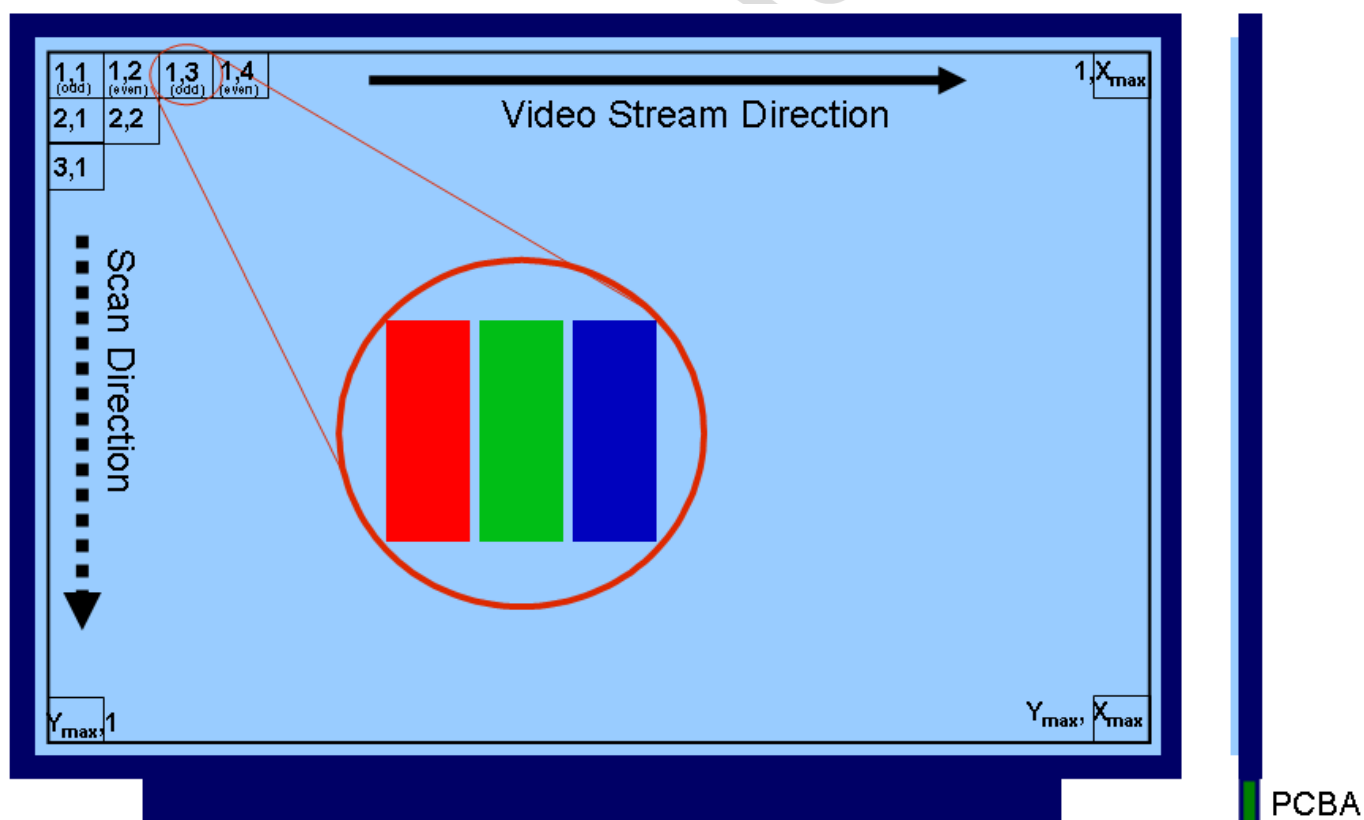
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	-
2	H_GND	High Speed Ground	-
3	Lane3_N	Complement Signal Link Lane 3	-
4	Lane3_P	True Signal Link Lane 3	-
5	H_GND	High Speed Ground	-
6	Lane2_N	Complement Signal Link Lane 2	-
7	Lane2_P	True Signal Link Lane 2	-
8	H_GND	High Speed Ground	-
9	Lane1_N	Complement Signal Link Lane 1	-
10	Lane1_P	True Signal Link Lane 1	-
11	H_GND	High Speed Ground	-
12	Lane0_N	Complement Signal Link Lane 0	-
13	Lane0_P	True Signal Link Lane 0	-
14	H_GND	High Speed Ground	-
15	AUX_CH_P	True Signal Auxiliary Channel	-
16	AUX_CH_N	Complement Signal Auxiliary Channel	-
17	H_GND	High Speed Ground	-
18	VCCS	LCD logic and driver power	-
19	VCCS	LCD logic and driver power	-
20	VCCS	LCD logic and driver power	-
21	VCCS	LCD logic and driver power	-
22	NC	No Connection (Reserved for LCD test)	-
23	GND	LCD logic and driver ground	-
24	GND	LCD logic and driver ground	-
25	GND	LCD logic and driver ground	-

26	GND	LCD logic and driver ground	-
27	HPD	HPD signal pin	-
28	BL_GND	Backlight ground	-
29	BL_GND	Backlight ground	-
30	BL_GND	Backlight ground	-
31	BL_GND	Backlight ground	-
32	LED_EN	Backlight on /off	-
33	LED_PWM	System PWM signal input for dimming	-
34	NC	No Connection (Reserved for LCD test)	-
35	NC	No Connection (Reserved for LCD test)	-
36	LED_VCCS	Backlight power	-
37	LED_VCCS	Backlight power	-
38	LED_VCCS	Backlight power	-
39	LED_VCCS	Backlight power	-
40	NC	No Connection (Reserved for LCD test)	-

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of BIST function are as follows.

Pin	Enable	Disable
BIST_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

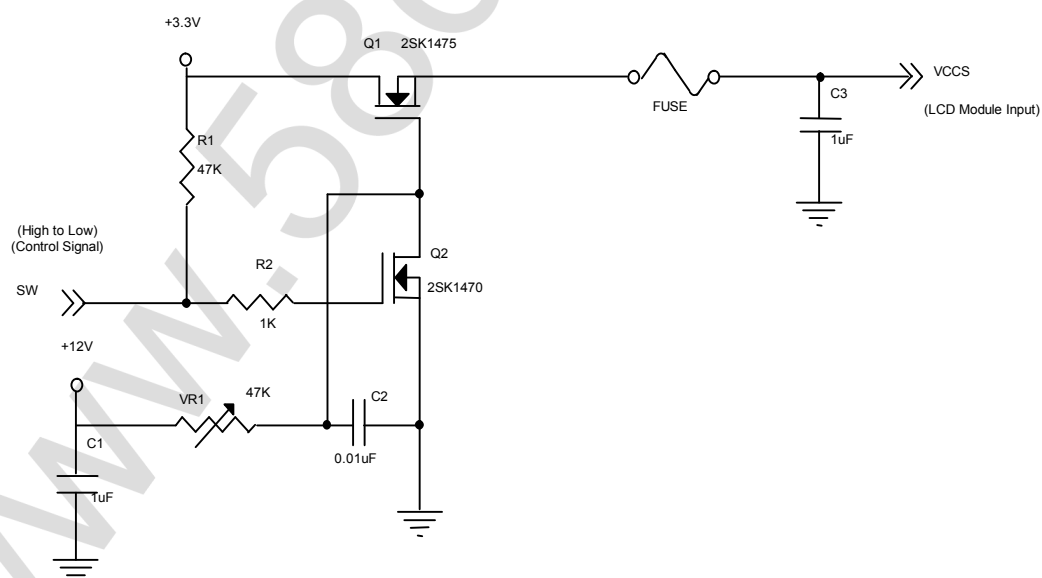
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
HPD	High Level	-	2.25	-	2.75	V	(6)
	Low Level	-	0	-	0.4	V	(6)
HPD Impedance		R_{HPD}	30K	-	-	ohm	(5)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
CABC_EN Input Voltage	High Level	V_{IHCABC}	2.3	-	3.6	V	(5)
	Low Level	V_{ILCABC}	0	-	0.5	V	(5)
CABC_EN Impedance		R_{CABC_EN}	30K	-	-	ohm	(5)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I_{CC}	-	(450)	(500)	mA	(3)a
	Black		-	(445)	(490)	mA	(3)
Power per EBL WG		P_{EBL}	-	(2.59)	-	W	(4)
Heavy Loading Pattern		I_{CC}	-	-	(900)	mA	-

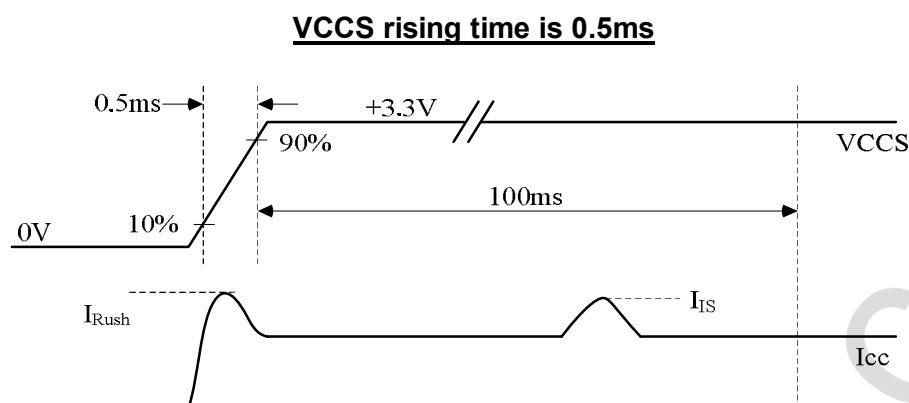
Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

Note (2) I_{RUSH} : the maximum current when VCCS is rising

I_{IS} : the maximum current of the first 100ms after power-on

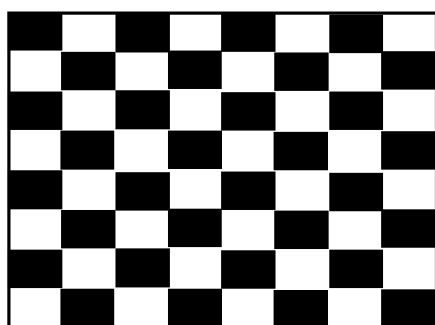
Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at $VCCS = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a specified power dissipation check pattern is displayed.

a. Mosaic Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) $VCCS = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, $f_v = 60\text{ Hz}$,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

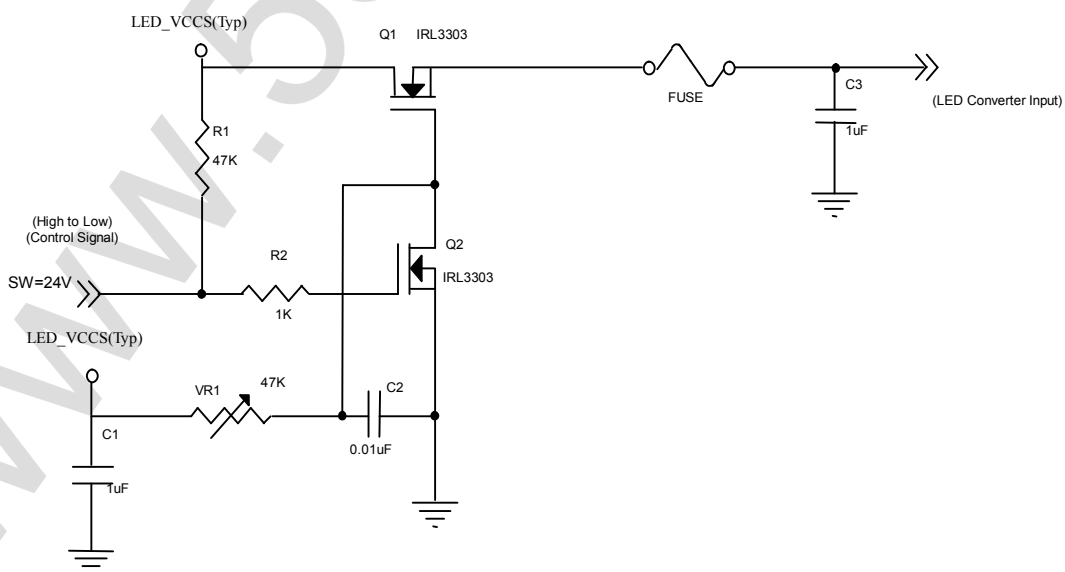
4.3.2 LED CONVERTER SPECIFICATION

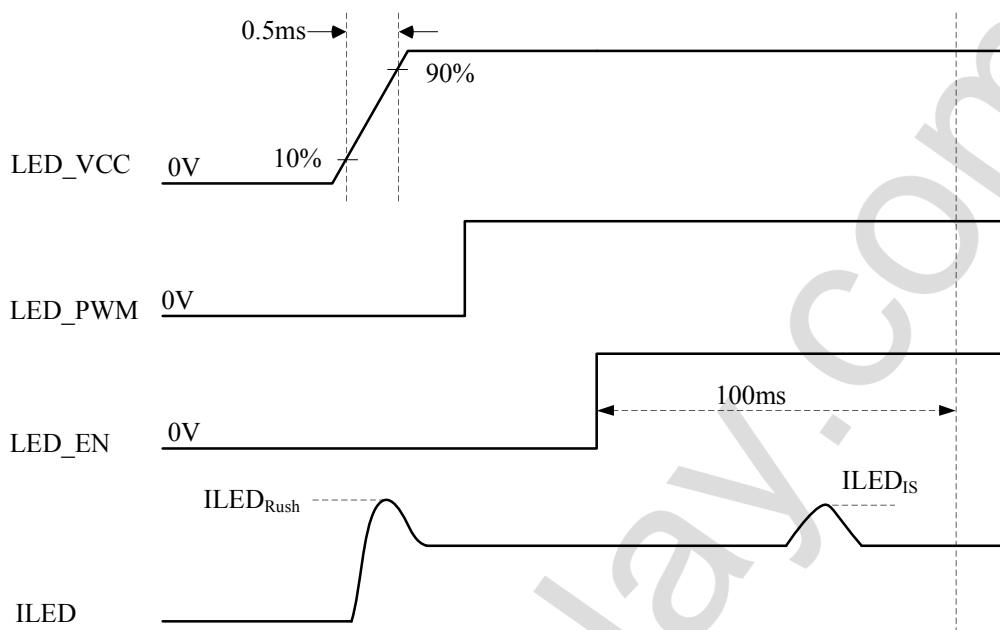
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	(8)	(12.0)	(21.0)	V	-
Converter Inrush Current		I _{LED_RUSH}	-	-	(1.5)	A	(1)
LED_EN Control Level	Backlight On	-	(2.2)	-	(5)	V	(4)
	Backlight Off		(0)	-	(0.6)	V	(4)
LED_EN Impedance		R _{LED_EN}	(30K)	-	-	ohm	(4)
PWM Control Level	PWM High Level	-	(2.2)	-	(5)	V	(4)
	PWM Low Level		(0)	-	(0.6)	V	(4)
PWM Impedance		R _{PWM}	(30K)	-	-	ohm	(4)
PWM Control Duty Ratio		-	(5)	-	(100)	%	(5)
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	(100)	mV	-
PWM Control Frequency		f _{PWM}	(190)	-	(2K)	Hz	(2)
LED Power Current	LED_VCCS =Typ.	I _{LED}	(807)	(933)	(969)	mA	(3)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms

Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

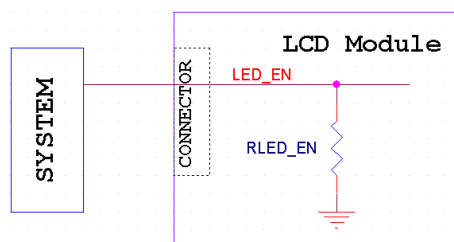
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM ...) are in the same concept.



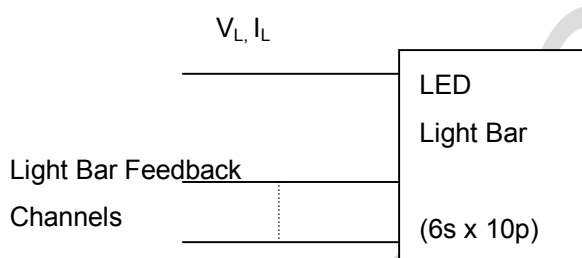
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V _L	33	33.9	35.4	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I _L	-	(270)	-	mA	
Power Consumption	P _L	-	(9.15)	(9.56)	W	(3)
LED Life Time	L _{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

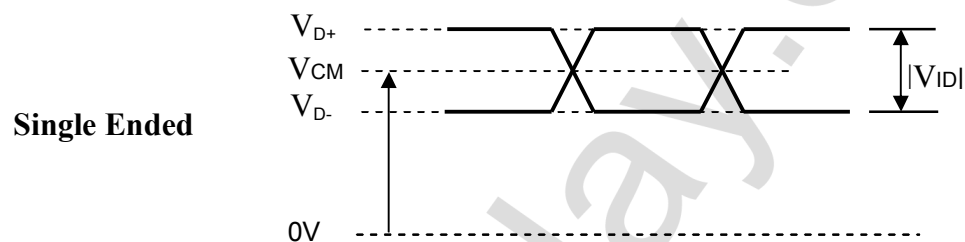
Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I_L = (27)mA (Per EA) until the brightness becomes ≤ 50% of its original value.

4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

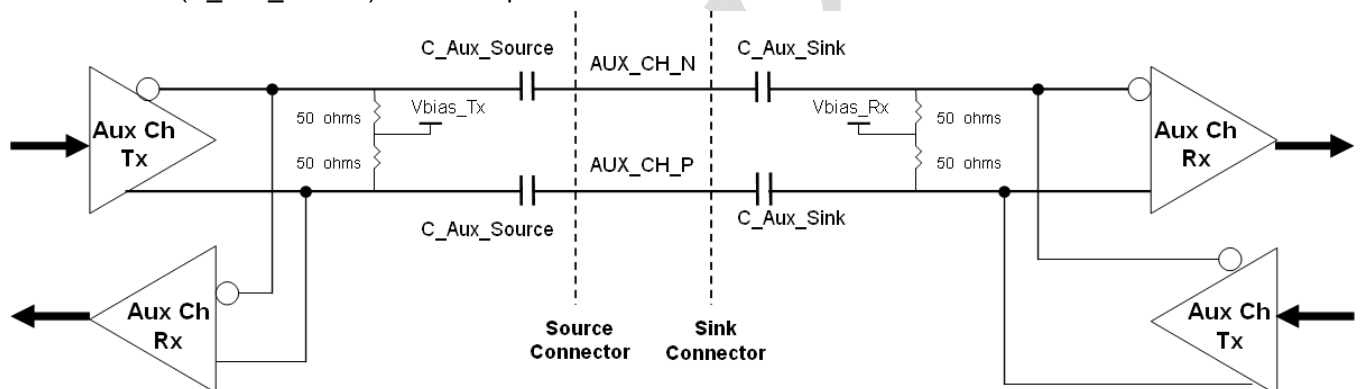
4.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0	-	2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75	-	200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75	-	200	nF	(3)

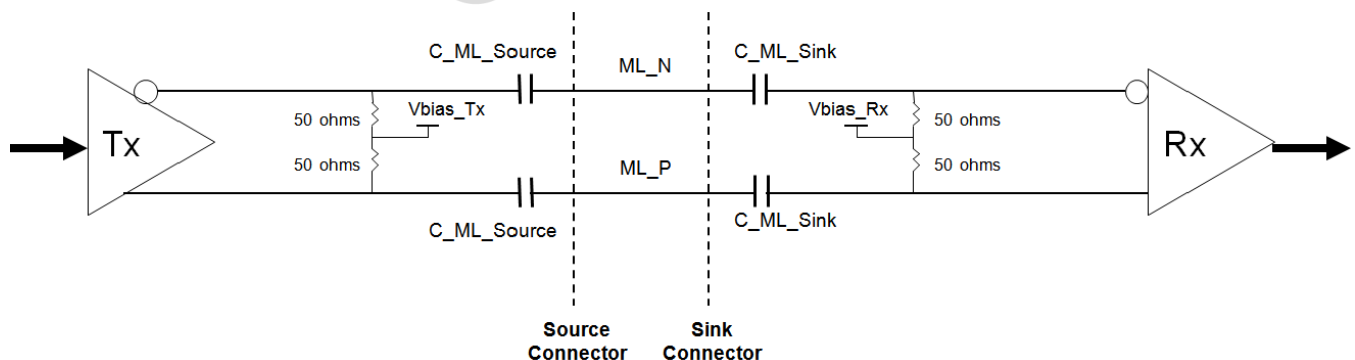
Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version 1.2. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_{ML Source}) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the **8-bit** gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
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	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

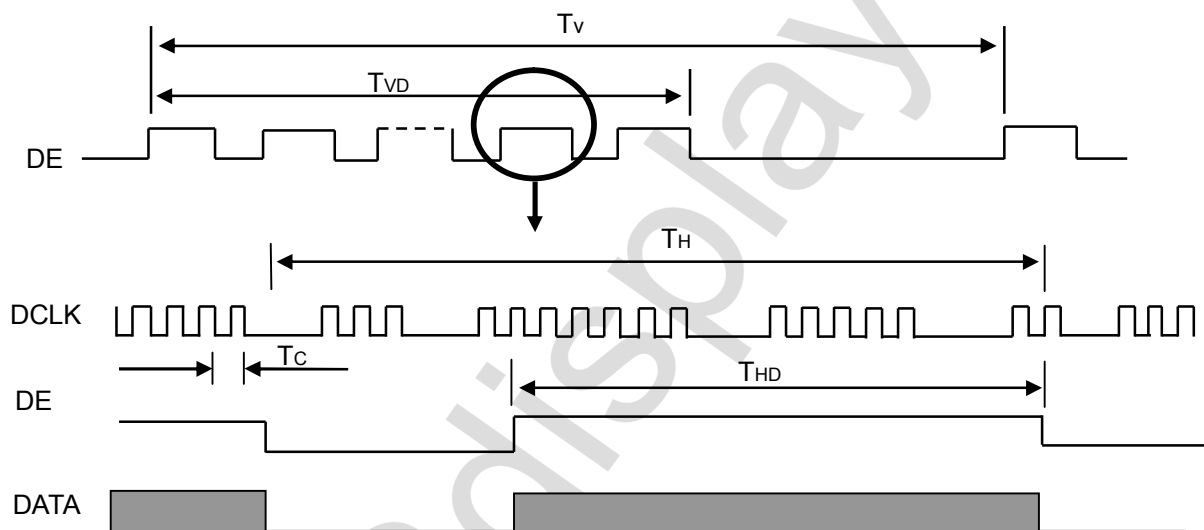
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

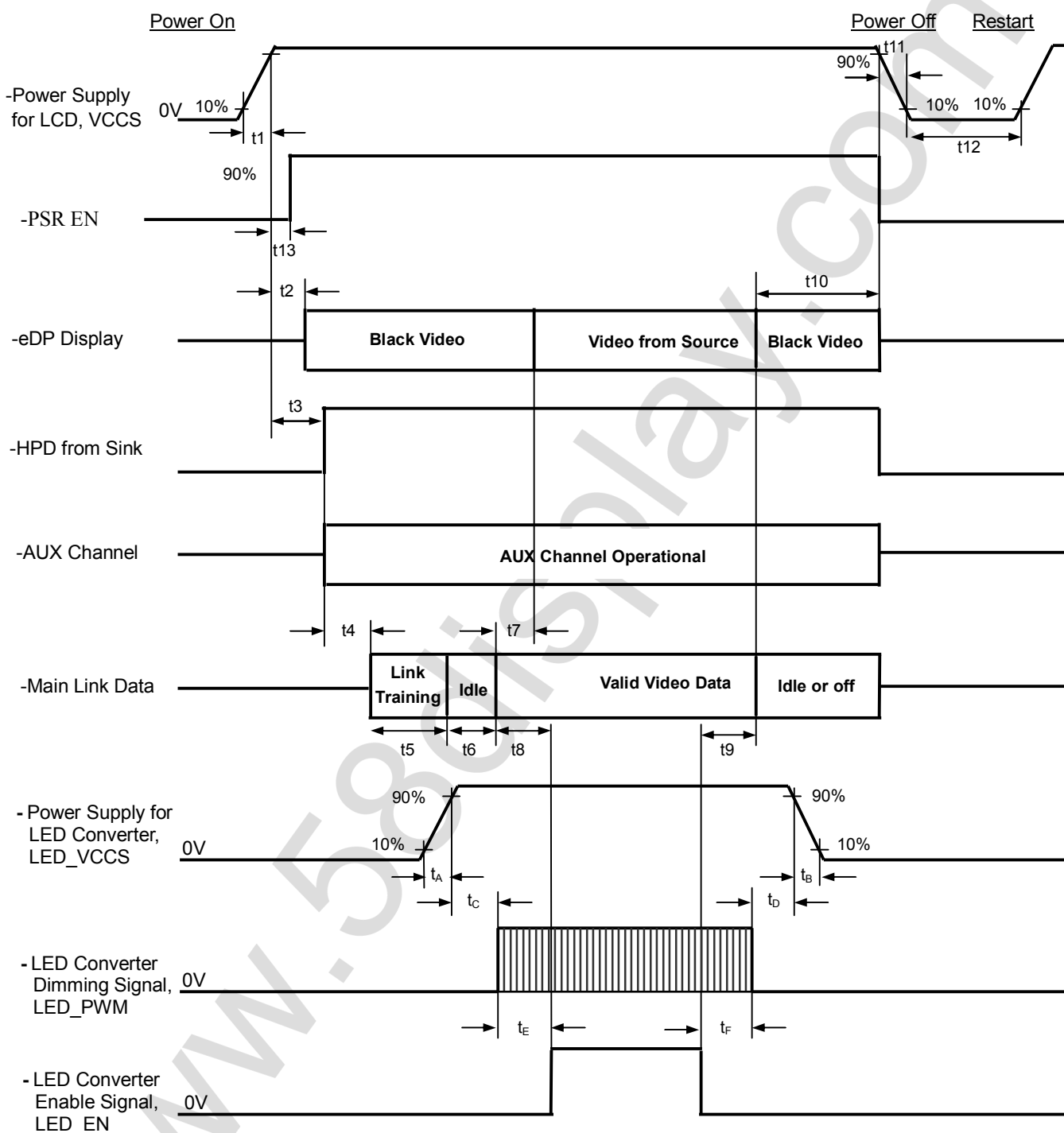
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	530.61	533.28	535.95	MHz	-
DE	Vertical Total Time	TV	2218	2222	2226	TH	-
	Vertical Active Display Period	TVD	2160	2160	2160	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	62	TV-TVD	TH	-
	Horizontal Total Time	TH	3980	4000	4020	Tc	-
	Horizontal Active Display Period	THD	3840	3840	3840	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	(0.5)	(10)	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	(0)	(200)	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	(0)	(200)	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	(0)	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	(0)	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	(0)	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	(0)	(50)	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	(80)	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	(50)	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	(0)	(500)	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	(0.5)	(10)	ms	-

t ₁₂	VCCS Power off time	Source	(500)	-	ms	-
t ₁₃	Delay from LCD,VCCS to PSR_EN high	Source	(0)	(5)	ms	PSR function select time
t _A	LED power rail rise time, 10% to 90%	Source	(0.5)	(10)	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	(0)	(10)	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	(1)	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	(1)	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	(0)	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	(0)	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T₂ max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T₉)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T₃ max. The panel's HPD may go high following LCDVCC(VCCS) power-on and goes low within 10ms, then the HPD stays low longer than 2ms. So, it must be regarded as a Hot-Plug/Unplug-Event. According to Section 5.1.4 of "VESA DisplayPort Standard", the source must read the link / sink status field and receiver capability field of the DPCD and re-train the link.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

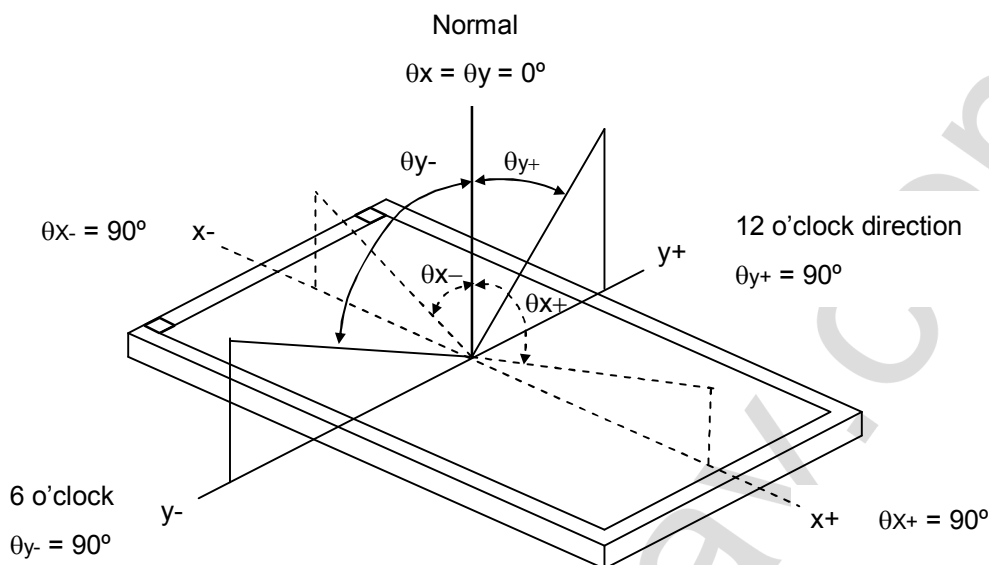
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	(270)	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	-	1200	-	-	(2), (5) ,(7)
Response Time		T _R		-	(16)	(19)	ms	(3) ,(7)
		T _F		-	(14)	(16)	ms	
Average Luminance of White		L _{Ave}		(510)	(600)	-	cd/m ²	(4), (6) ,(7)
Color Chromaticity	Red	R _x		Typ – 0.03	(0.640) (0.330) (0.210) (0.710) (0.150) (0.060) (0.313) (0.329)	Typ + 0.03	-	(1) ,(7)
		R _y					-	
	Green	G _x					-	
		G _y					-	
	Blue	B _x					-	
		B _y					-	
	White	W _x					-	
		W _y					-	
	Color Gamut	C.G.					-	
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5) , (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation		δW _{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	-	-	1.25	%	(5),(6) ,
		δW _{13p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	-	1.4	1.6	%	(7)

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

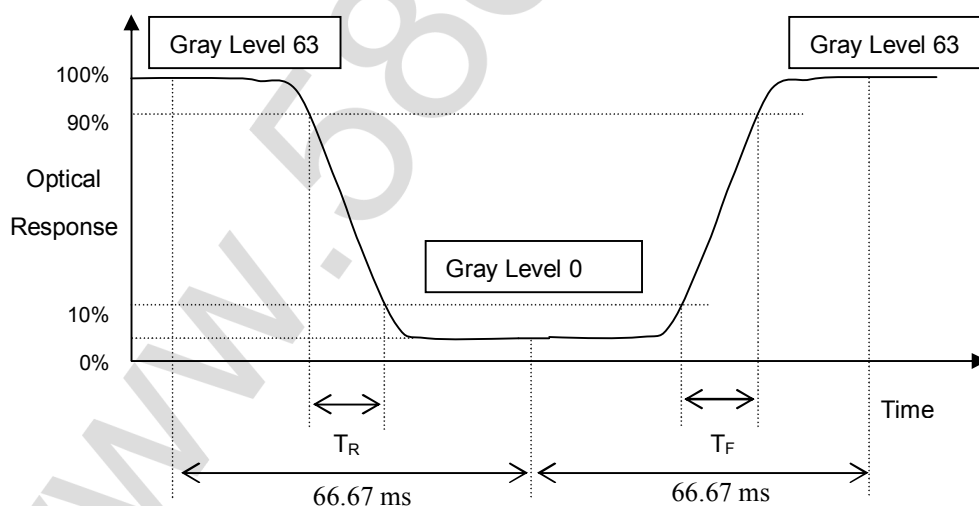
L_{63} : Luminance of gray level 63

L_0 : Luminance of gray level 0

$$CR = CR(1)$$

$CR(X)$ is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

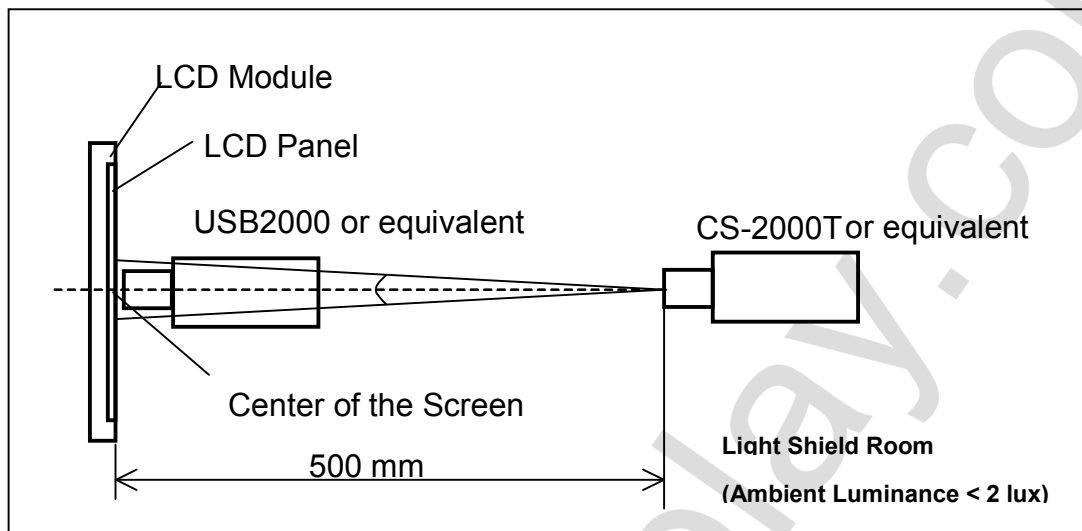
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

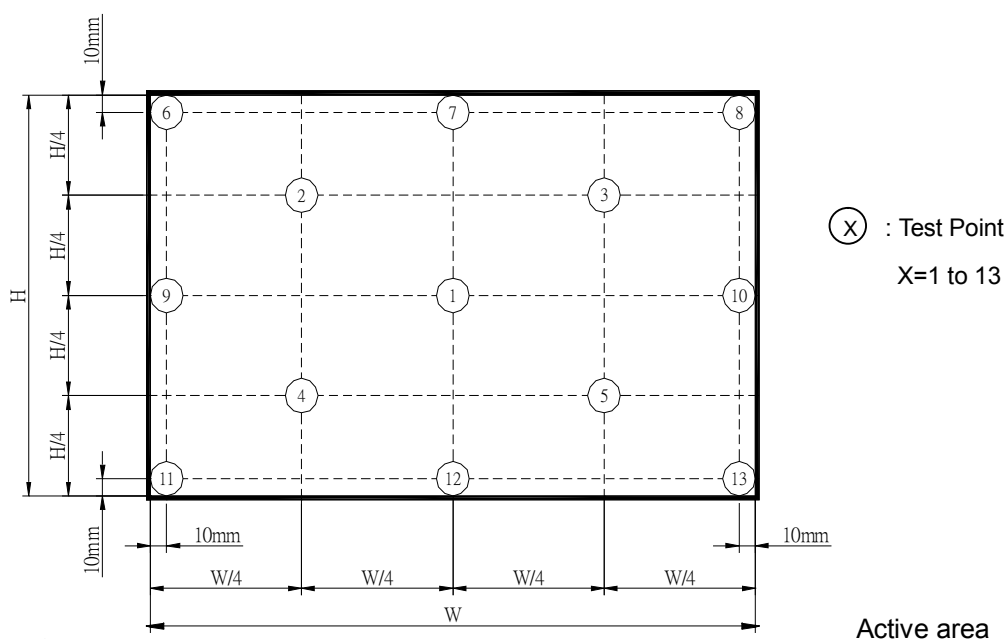
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \{ \text{Maximum } [L(1) \sim L(5)] / \text{Minimum } [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Maximum } [L(1) \sim L(13)] / \text{Minimum } [L(1) \sim L(13)] \} * 100\%$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

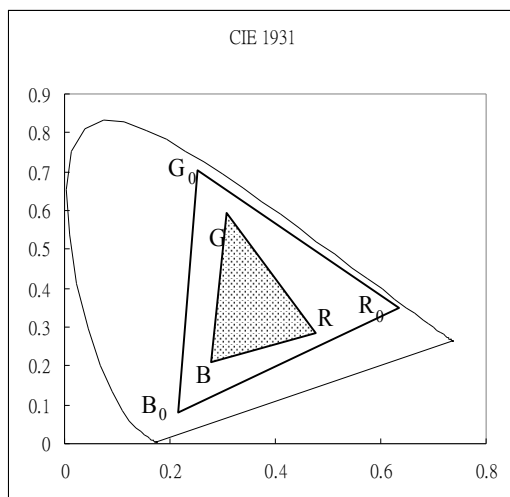
$$C.G\% = \text{Area}(R, G, B) / \text{Area}(R_0, G_0, B_0) * 100\%$$

R_0, G_0, B_0 : CIE1931 coordinates of red, green, and blue defined by NTSC.

R, G, B : CIE1931 coordinates of red, green, and blue in module at 255 gray level.

$\text{Area}(R_0, G_0, B_0)$: Area of the triangle defined by coordinate R_0, G_0, B_0 .

$\text{Area}(R, G, B)$: Area of the triangle



defined by coordinate R, G, B

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour \longleftrightarrow 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, RH 80%, 240hours	(1)
ESD Test (Operation)	150pF, 330 Ω , 1sec/cycle Condition 1 : Contact Discharge, $\pm 8KV$ Condition 2 : Air Discharge, $\pm 15KV$	
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of $\pm X, \pm Y, \pm Z$	
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	

Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N156DCE – GN2
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: XXXXXXYMDLNNNN
 - Serial No.
 - Product Line
 - Year, Month, Date
 - INX Internal Use
 - Revision
 - INX Internal Use

- (d) Production Location: MADE IN XXXX.
- (e) UL Logo : XXXX or XXXXX is UL factory ID.

Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

7.2 CARTON

- (1) Box Dimensions : 500(L)*370(W)*270(H)
 (2) 20 modules/Carton

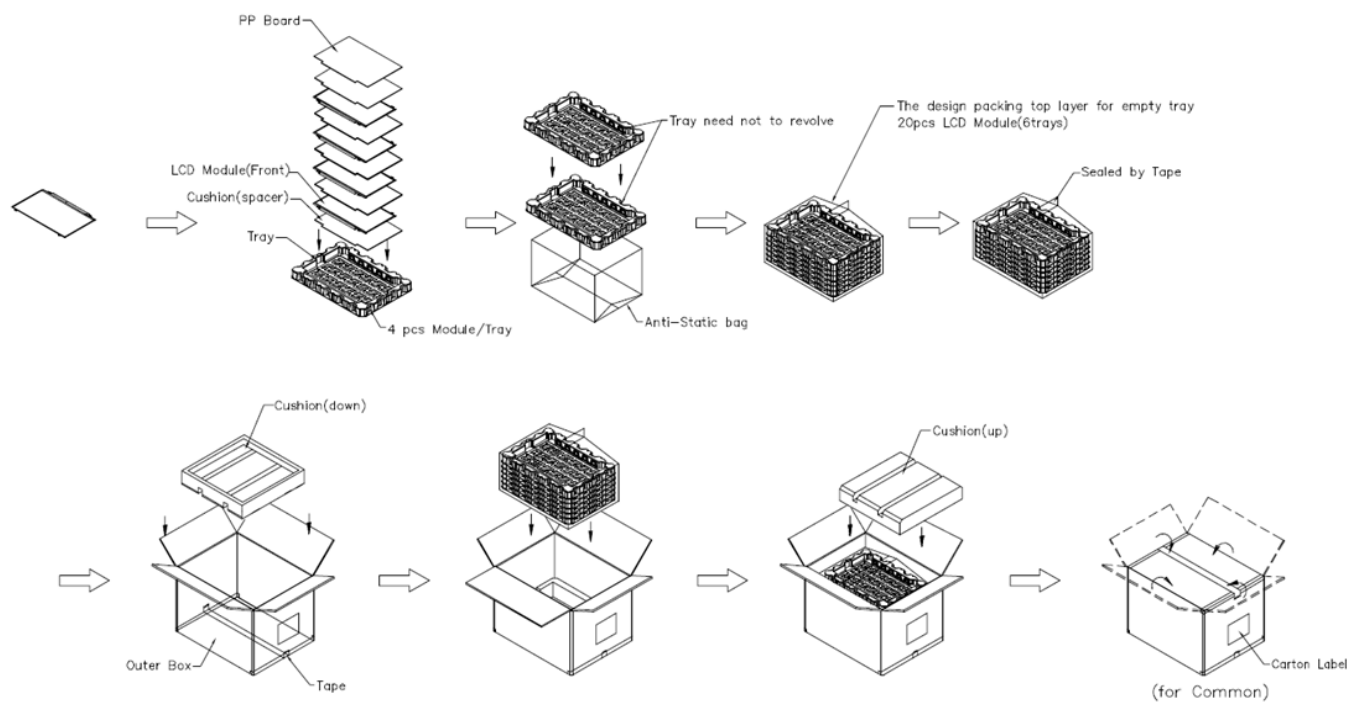


Figure. 7-1 Packing method

7.3 PALLET

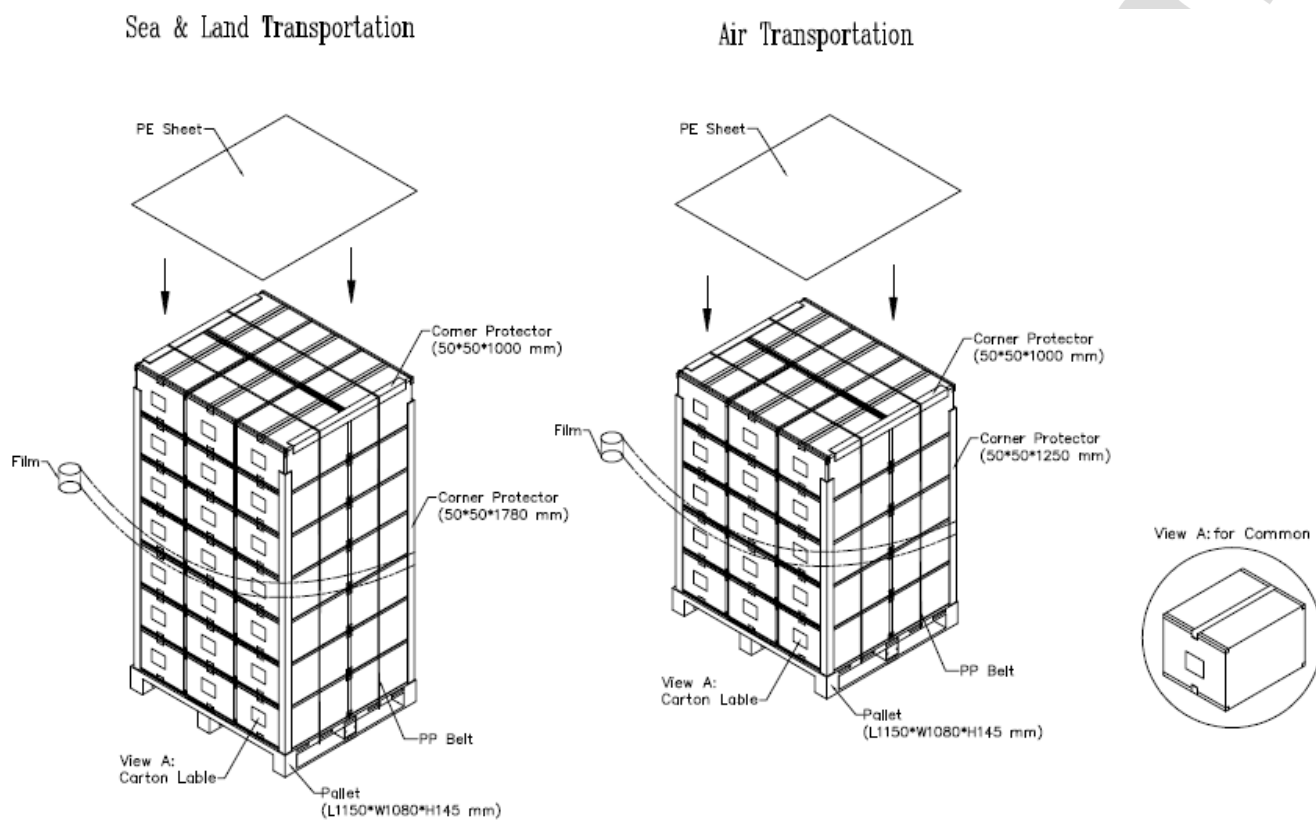


Figure. 7-2 Packing method

7.4 UN-PACKAGING METHOD

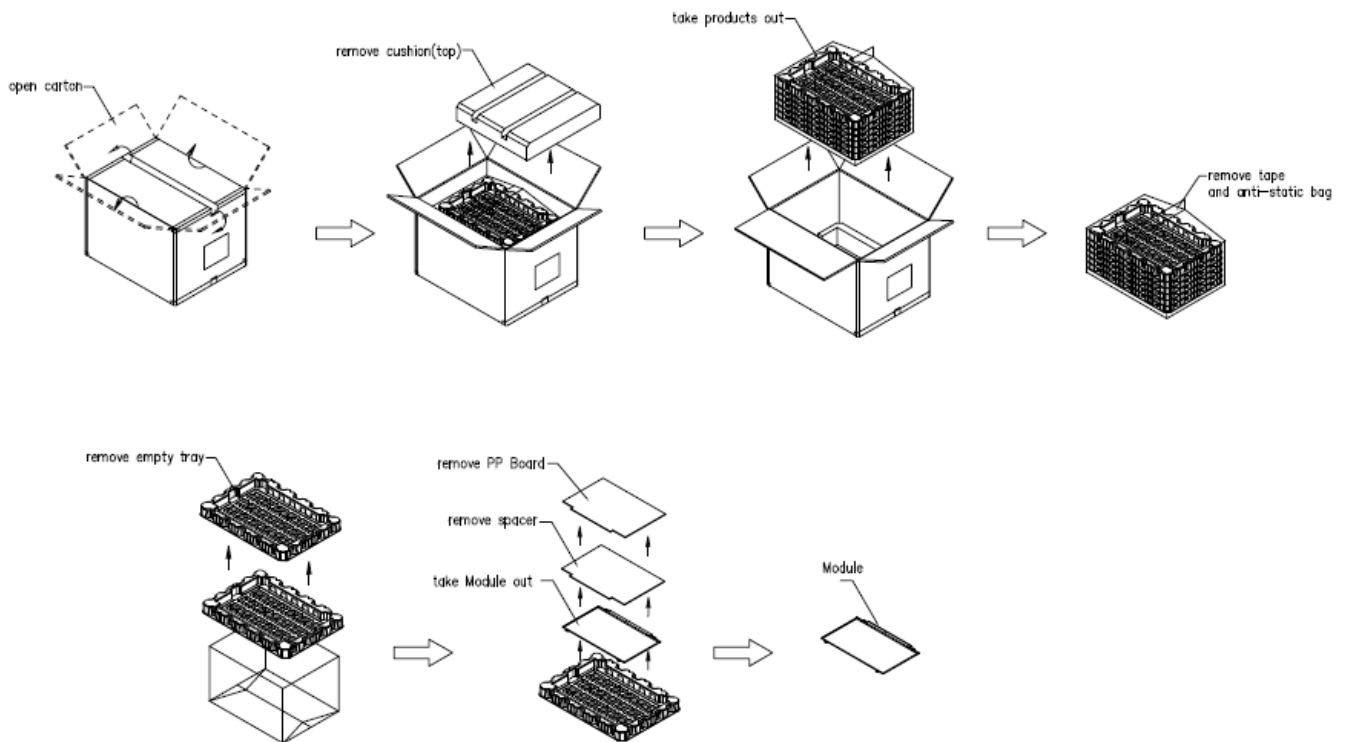


Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.
- (12) Do not re-attach protective film onto the polarizer because of risk of bubble mura and dust.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

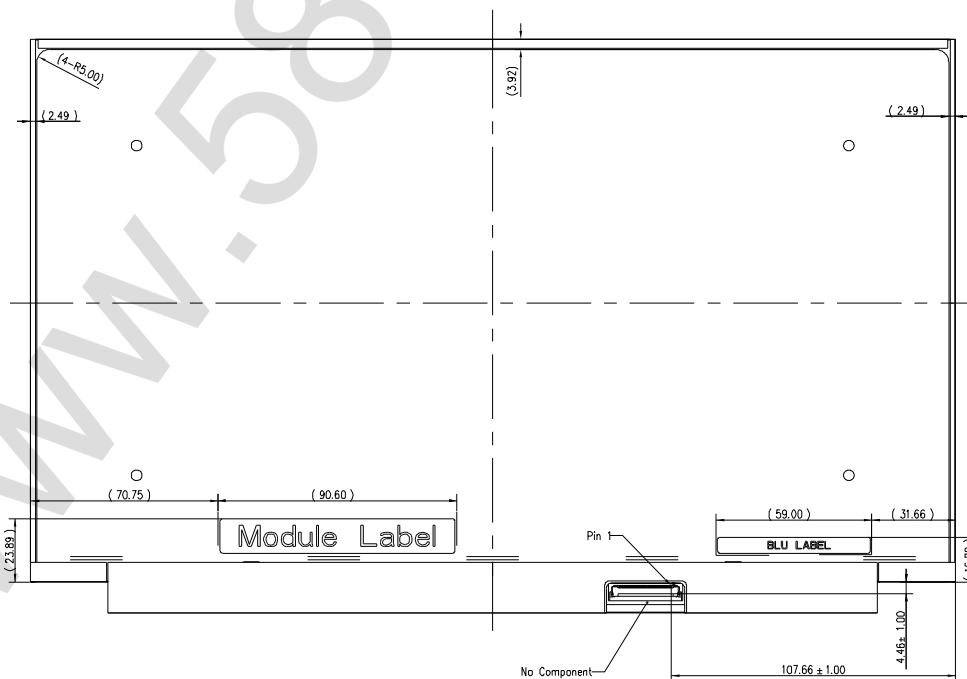
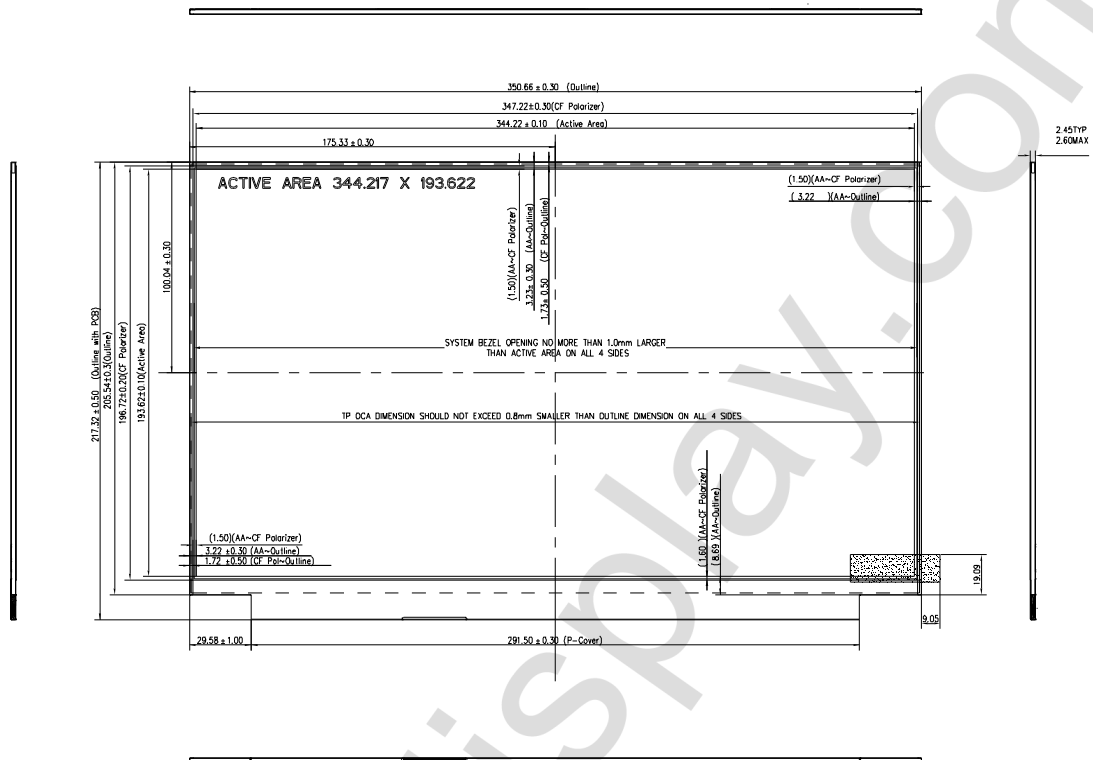
- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

[illegible]

[illegible]

[illegible]

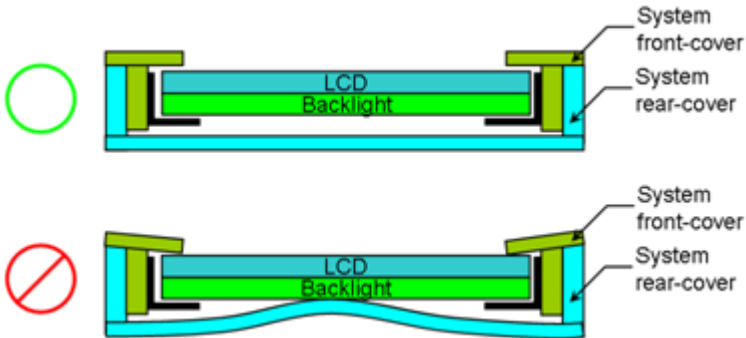
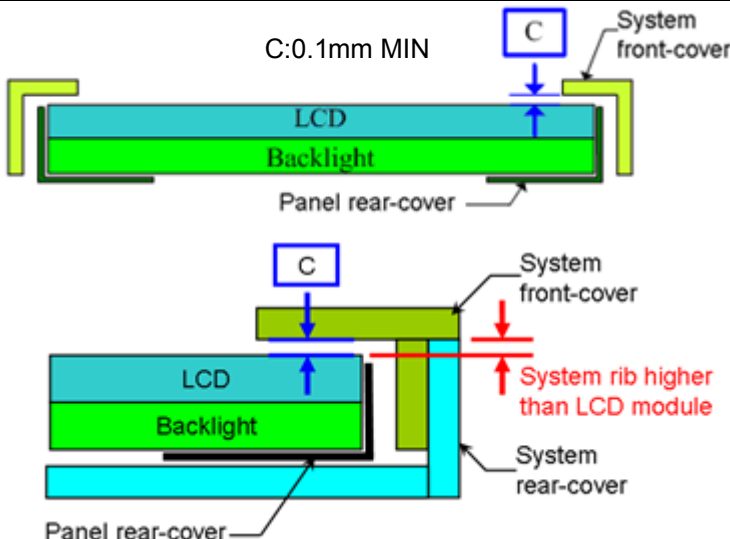
Appendix. OUTLINE DRAWING

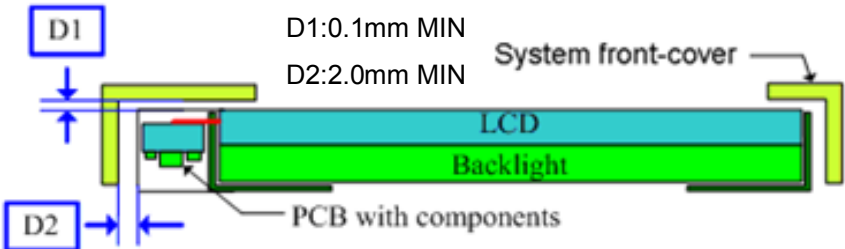
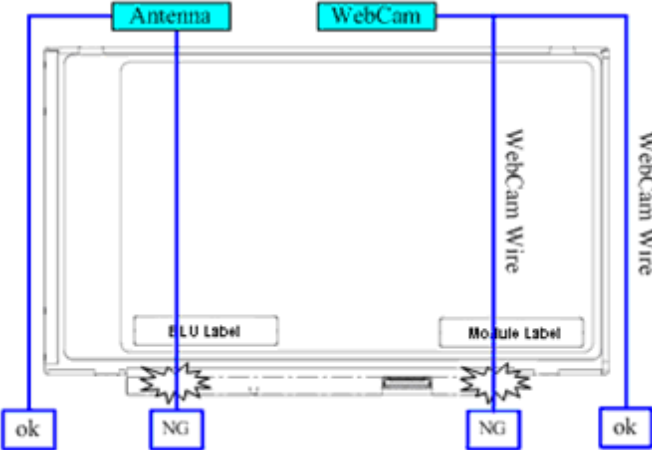


NOTES:

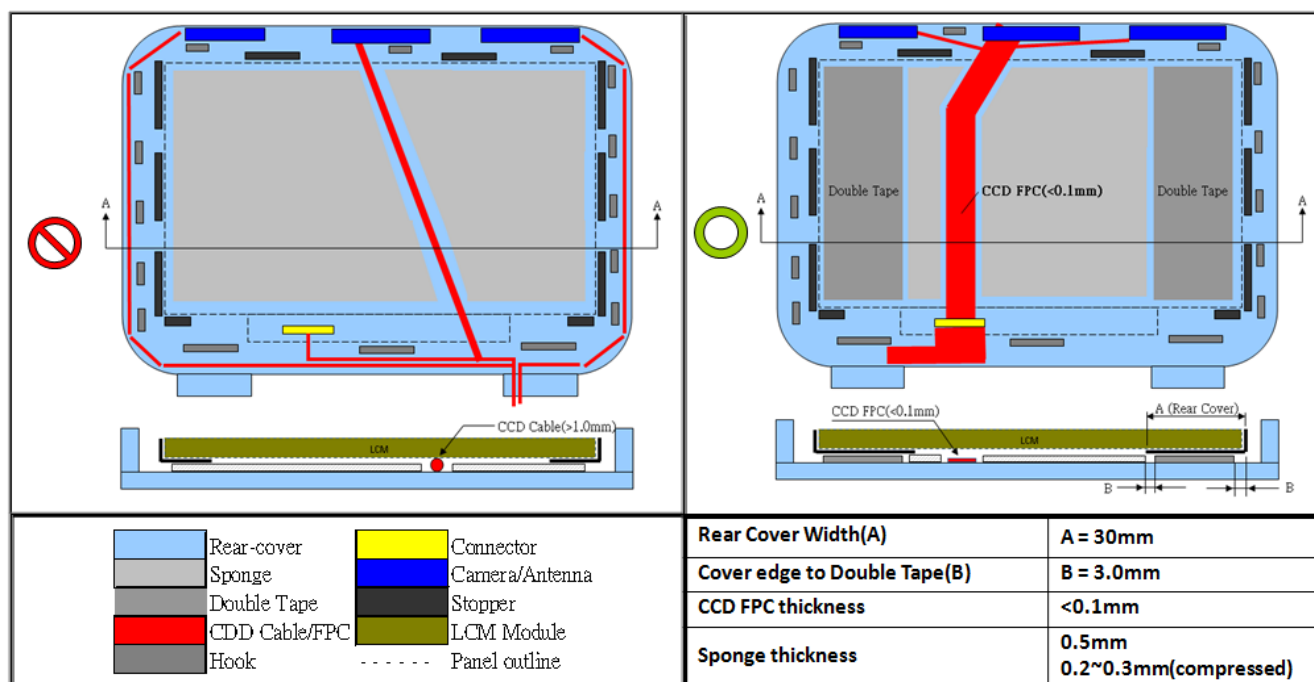
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SOFT,
NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR
FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN 1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC (0.5mm) MAX. (SPEC WILL BE MODIFIED AFTER DVT CHECK).
4. "()" MARKS THE REFERENCE DIMENSION.

Appendix. SYSTEM COVER DESIGN NOTICE

0.	Permanent deformation of system cover after reliability test
	 <p>System front-cover System rear-cover LCD Backlight</p>
Definition	<p>System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.</p> <p>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>
1	Design gap C between system front-cover & panel surface.
	 <p>C:0.1mm MIN C System front-cover LCD Backlight Panel rear-cover System front-cover System rear-cover LCD Backlight System rib higher than LCD module Panel rear-cover</p>
Definition	<p>Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.</p> <p>To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>
2	Design gap D1 & D2 between system front-cover & PCB Assembly.

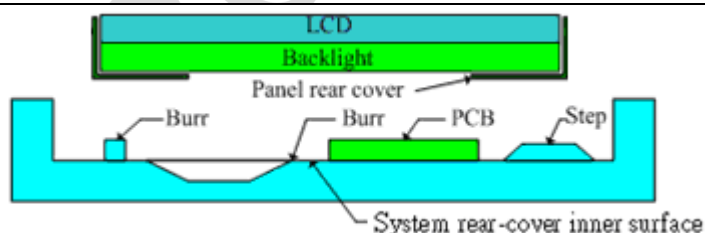
 <p>D1: 0.1mm MIN D2: 2.0mm MIN</p> <p>System front-cover</p> <p>LCD</p> <p>Backlight</p> <p>PCB with components</p>	
Definition	Same as point 2 and 3, but focus on PCBA side.
3	Interference examination of antenna cable and WebCam wire
	
Definition	<p>Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur.</p> <p>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>
4	Interference examination of antenna cable and Web Cam wire

- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.



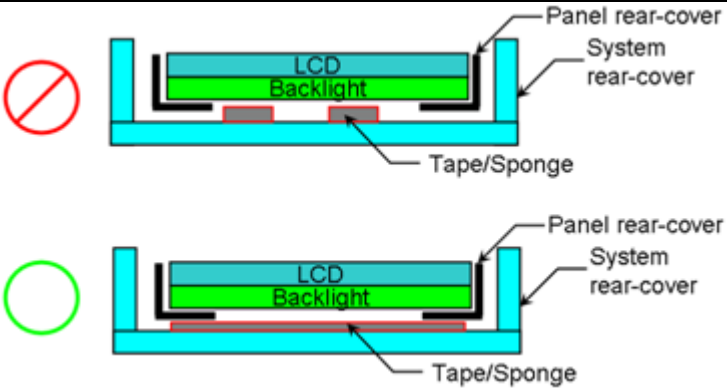
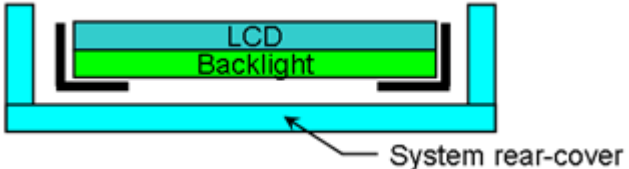
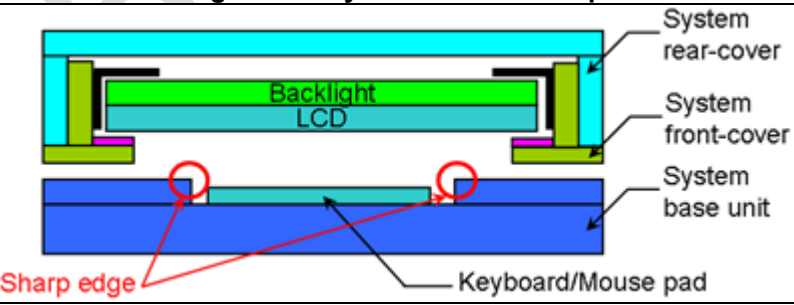
If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC)
 Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

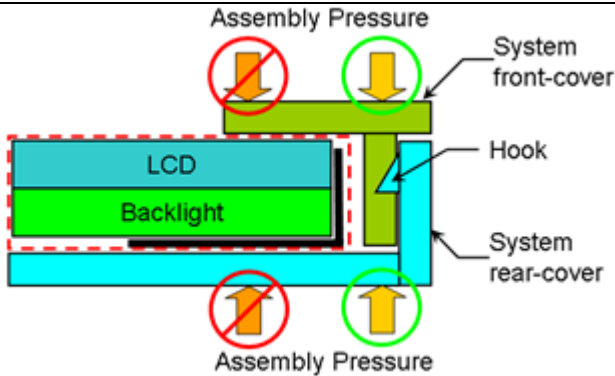
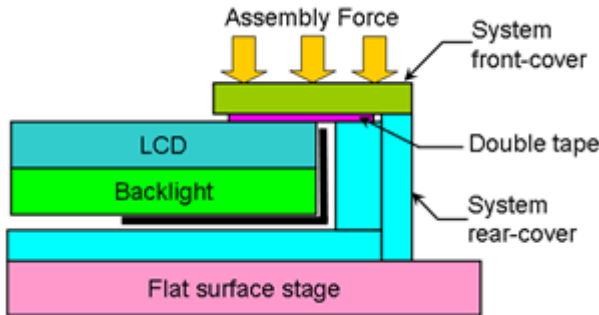
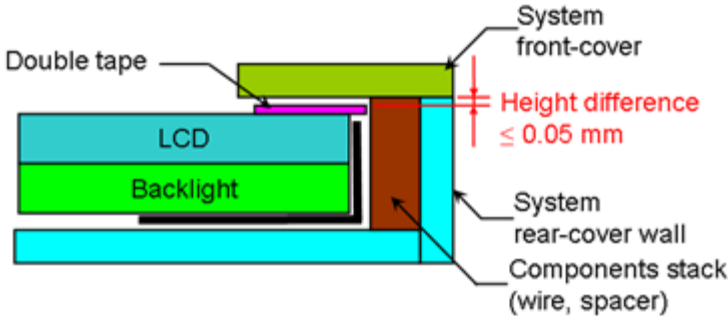
5 System rear-cover inner surface examination

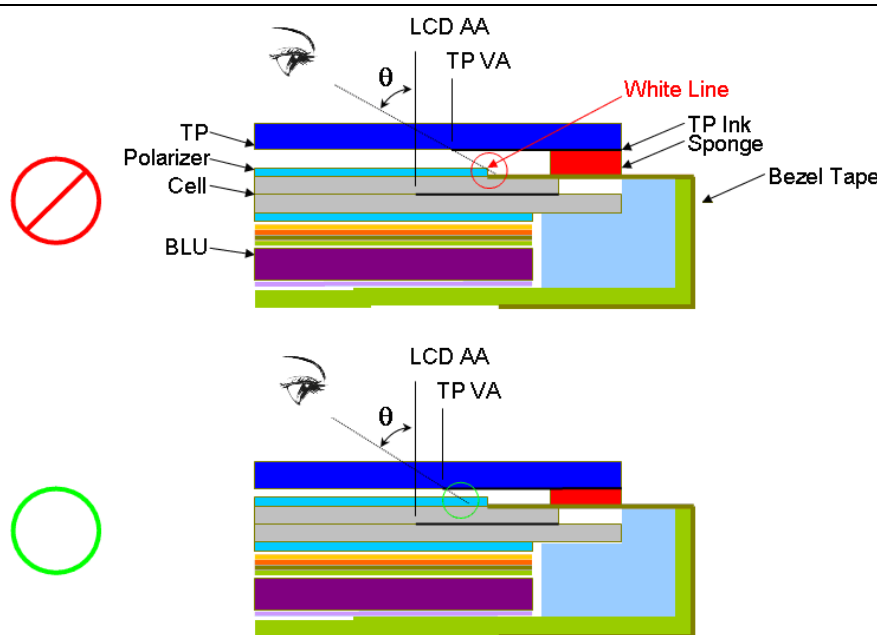


Definition Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.

6 Tape/sponge design on system inner surface

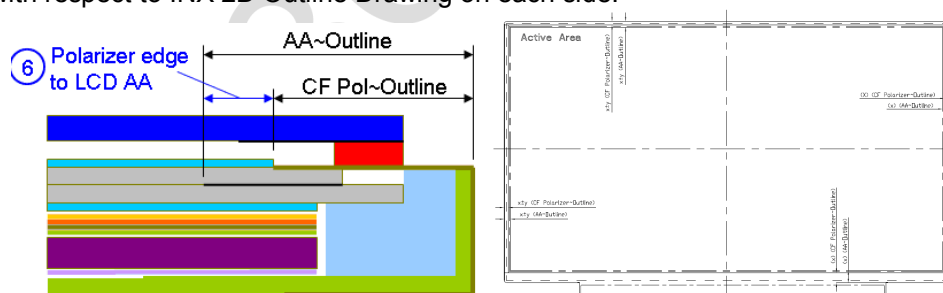
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7	Material used for system rear-cover
 <p>System rear-cover material: Al-Mg alloy System rear-cover thickness: 1.5mm MIN</p>	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
8	System base unit design near keyboard and mouse pad
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
9	Assembly SOP examination for system front-cover with Hook design

	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
10	Assembly SOP examination for system front-cover with Double tape design
	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm ²) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.
11	System front-cover assembly reference with Double tape design
	
Definition	To prevent system front-cover peeling at double tape contact area, Height difference between system front-cover assembly reference such as wall or components stack (wire, spacer) and double tape top surface must be less than 0.05mm.
12	Touch Application : TP and LCD Module Combination for White Line Prevention

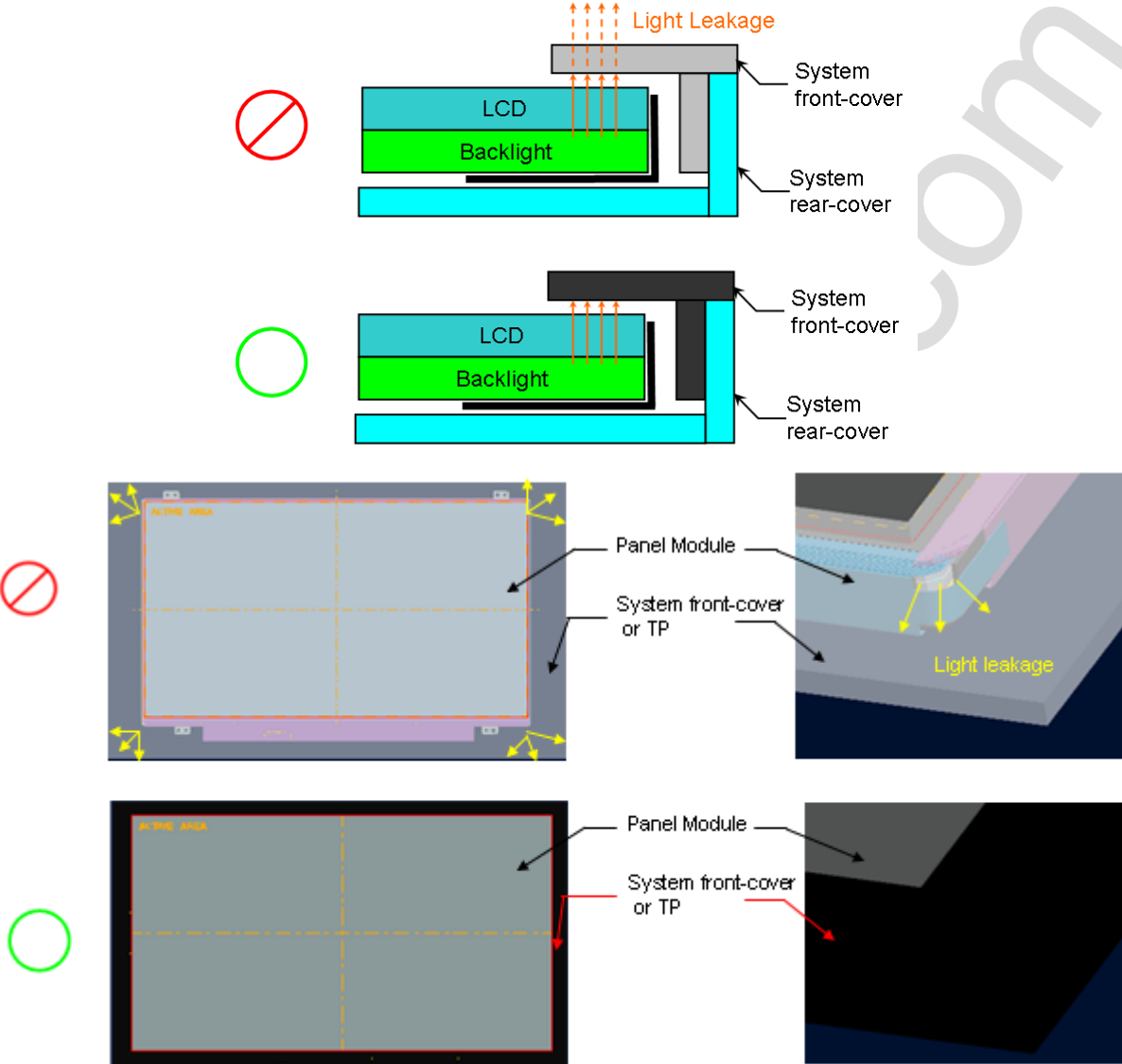
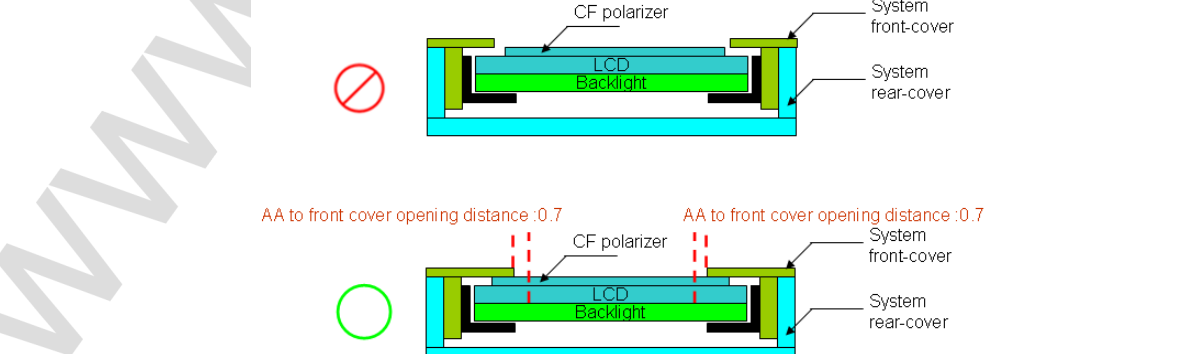

Parameter consideration for White Line Issue :

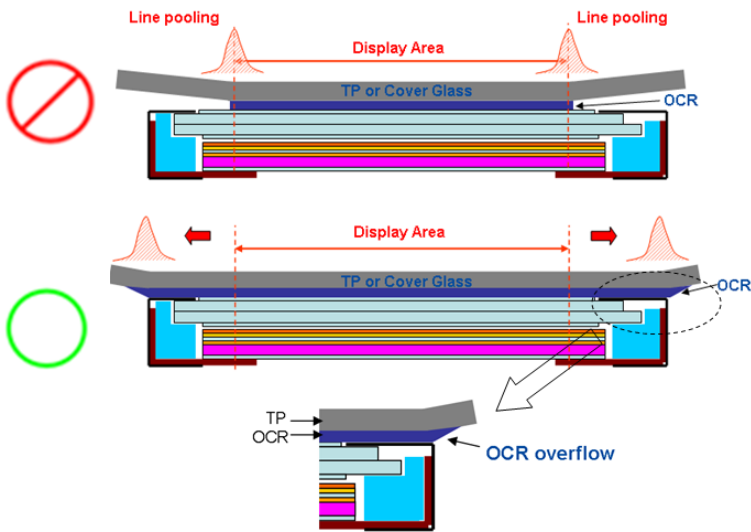
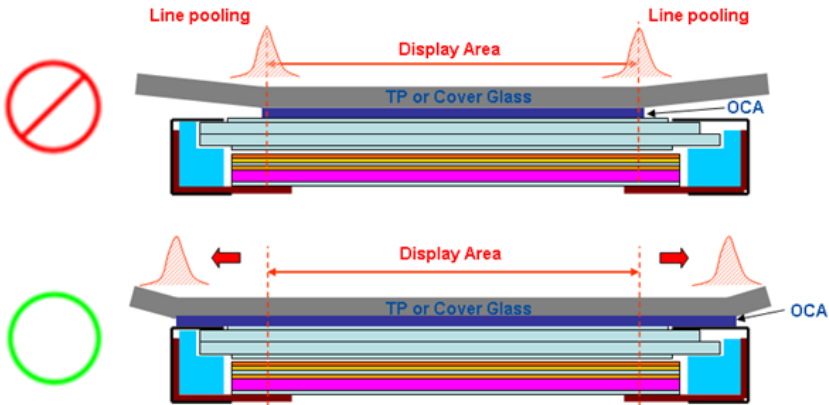
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side.




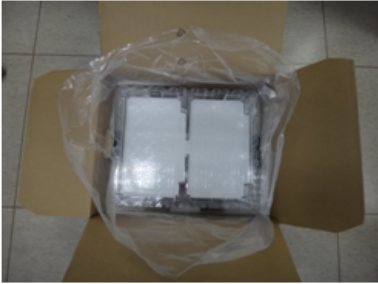




Definition	<p>For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear.</p> <p>Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately.</p> <p>The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area.</p> <p>Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline").</p> <p>Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.</p>
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13	Color of system front-cover material
	 <p>The diagrams illustrate the importance of using dark-colored material for the system front-cover to prevent light leakage. The top section shows a cross-section of the LCD assembly (LCD and Backlight) between the system front-cover and rear-cover. A red 'X' indicates that a transparent front-cover allows light to leak out, while a green circle indicates that a dark front-cover prevents this. The bottom section shows a top-down view of the panel module with the active area and the distance from the active area to the front cover opening (AA to front cover opening distance) marked. A red 'X' shows light leakage from the edges of the panel when the front cover is transparent, while a green circle shows no leakage when the front cover is dark.</p>
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
14	AA to front cover opening distance
	 <p>The diagrams illustrate the requirement for the distance from the active area (AA) to the front cover opening. The top section shows a cross-section of the LCD assembly (LCD, Backlight, and CF polarizer) between the system front-cover and rear-cover. A red 'X' indicates that a large opening allows light to leak out. The bottom section shows a cross-section with the 'AA to front cover opening distance' specified as 0.7mm, marked with red dashed lines. A green circle indicates that this distance is correct to prevent leakage.</p>
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.

15	Use OCR Lamination
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
16	Use OCA Lamination
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	<ul style="list-style-type: none"> • This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure. • This manual provides guide in unpacking and handling steps. • Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.
1.	Unpacking
<div style="display: flex; flex-direction: column; align-items: center;"> <div style="display: flex; justify-content: space-around; width: 100%;"> <div style="text-align: center;">  </div> <div style="text-align: center;">  <p>Open carton</p> </div> <div style="text-align: center;">  <p>Remove EPE Cushion</p> </div> </div> <div style="margin: 10px 0;">↓</div> <div style="display: flex; justify-content: space-around; width: 100%;"> <div style="text-align: center;">  <p>Open plastic bag</p> </div> <div style="text-align: center;">  <p>Cut Adhesive Tape</p> </div> <div style="text-align: center;">  <p>Remove EPE Cushion</p> </div> </div> </div>	
2.	Panel Lifting

Remove PET Cover



Remove PE Foam

Handle with care
(see next page)

Finger Slot

Use slots at both sides for finger insertion.
Handle panel upward with care.

3.

Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.



Don't :

- Lifting with one hand.

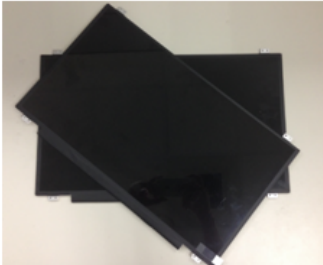


- Handle at PCBA side.



Don't :

- Stack panels.



- Press panel.



Don't :

- Put foreign stuff onto panel



- Put foreign stuff under panel



Don't :

- Paste any material unto white reflector sheet



Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.



Don't :

- Twist panel.



Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.



Do :

- Remove panel protector film starts from pull tape



Don't :

- Remove panel protector film From film another side.



Don't :

- Touch or Press PCBA Area.

